

1. For the following state table,

q	q *		z	
	x = 0	x = 1	x = 0	x = 1
A	B	C	1	1
B	A	D	0	1
C	B	A	0	0
D	C	C	1	1

a) Draw a state diagram.

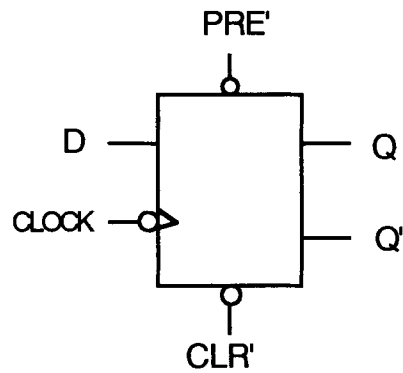
b) Complete the following timing trace as far as you can, even after you no longer know the input.

x    0    0    1    0    1

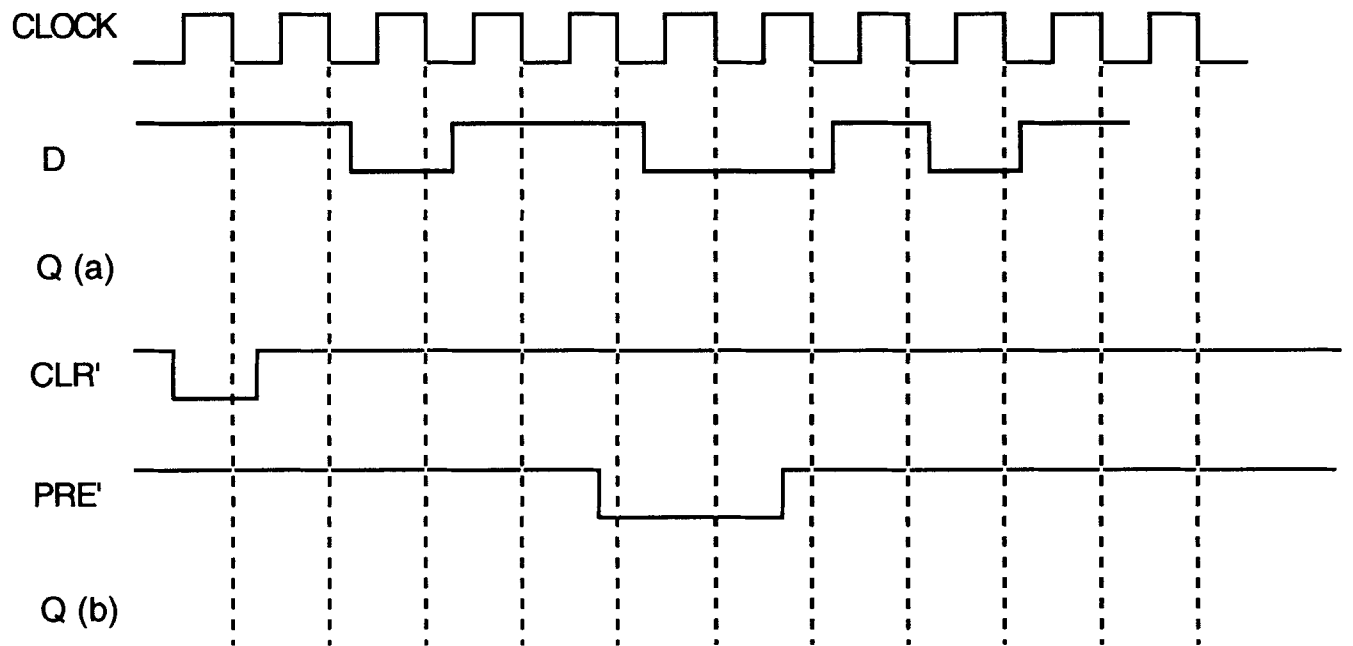
q    A

z

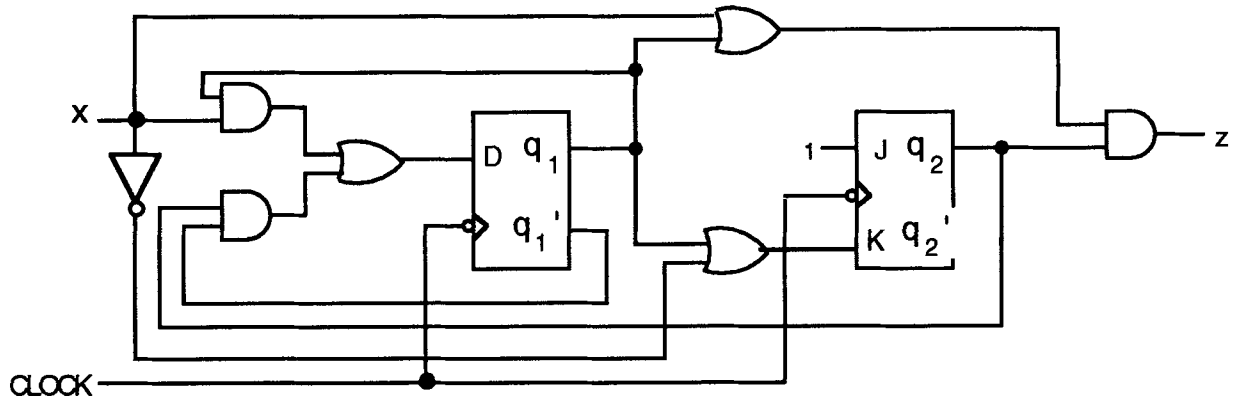
2. For the trailing-edge triggered D flip flop shown, complete the timing diagram (showing Q for as far as you can).



- a) If there is no CLR' or PRE'.
- b) With the values of CLR' and PRE' shown (same D as in part a)

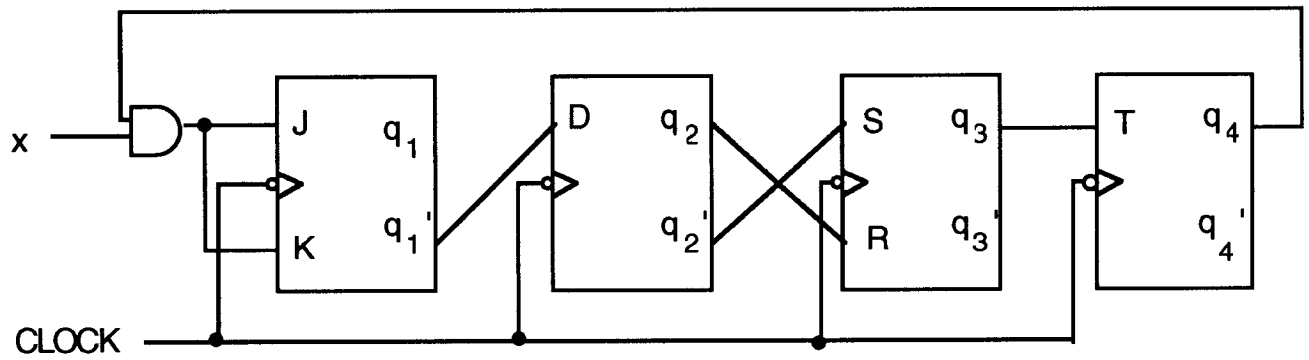


3. For the circuit shown (with trailing-edge triggered flip flops), complete the state table.



$q_1 q_2$	$q_1^* q_2^*$		$z$	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0 0				
0 1				
1 0				
1 1				

4. For the following circuit, complete the timing trace as far as you can, even after the input is no longer known.



x	0	0	1	1	0	1
q <sub>1</sub>	0					
q <sub>2</sub>	0					
q <sub>3</sub>	0					
q <sub>4</sub>	0					